IN THE DRAWINGS

Formal drawings including FIG. 1A, FIG. 1B, FIG. 1C, FIG. 1D, FIG. 2, FIG. 3, FIG. 4, FIG. 5, and FIG. 6 on sheet 1-6 are provided with this response. Each of sheets 2-5 has been labeled as "REPLACEMENT SHEET" in the title of each sheet. Each of sheets 1 and 6 has been labeled as "ANNOTATED SHEET" in the title of each sheet.

FIG. 1A is marked to include the proposed amendments adding the labels: "NIBBLE 7" "NIBBLE 6" "NIBBLE 5" "NIBBLE 4" "NIBBLE 3" "NIBBLE 2" "NIBBLE 1" and "NIBBLE 0".

FIG. 1B is marked to include the proposed amendments adding labels: "BYTE 3" "BYTE 2" "BYTE 1" and "BYTE 0".

FIG. 1C is marked to include the proposed amendments adding labels: "HALF-WORD 1" and "HALF-WORD 0".

FIG. 6 is marked to include the proposed amendments to blocks 520, 540, and 560.

REMARKS

Claims 1, 7, 12, and 17 are amended, claims 23-25 are added, and no additional claims are cancelled in this response. Claims 20-22 were previously canceled. As a result, claims 1-19 and 23-25 are pending in this application.

No new matter has been added through the amendments to claims 1, 7, 12, and 17. Claims 1, 7, 12, and 17 were each amended in part wherein the phrase "the status" was amended to read "a status" in order to provide a proper antecedent basis for "status" in claims 1, 7, 12, and 17.

In addition, claims 1, 7, and 12 were amended to add the word "logically" to each of these claims, and claim 17 was amended to add the phrase "the plurality of arithmetic flags associated with a single selected data item" to claim 17. Support for these amendments to claims 1, 7, 12, and 17 may be found throughout the specification, including but not limited to the specification at page 6, line 15 through page 7, line 14, and page 9, line 18 through page 10, line 9.

Further, no new matter has been added through new claims 23-25. Support for new claims 23-25 may be found throughout the specification as originally filed, including but not limited to the specification on page 6, line 15 through page 7, line 14, FIG. 2, and claim 1 as originally filed.

Specification Objections

Regarding the title.

The title of the application was deemed to be not descriptive by the Examiner. The title has been amended in order to make the title more descriptive and to more accurately reflect the content of the independent claims. Therefore, Applicant respectfully requests notification that the objection to the title is withdrawn.

Regarding the specification on page 13, lines 2-10.

The Final Office Action on page 2 states, "On page 13, lines 2-10, steps 520 and 540 should be explained more clearly."

Applicant believes that the statements made on page 2 in the Final Office Action with respect to the above mentioned portion of the specification has merit. Applicant believes that the specification discloses an extraction wherein based on the determined field size, a plurality of specified destination register bits in a destination register are set to the arithmetic flags associated with a selected and specific data item. The number of the plurality of specific destination register bits set, and the number of arithmetic flags used in setting these bits matches the determined field size, for example but not limited to a field size reprehensive of a nibble, a byte, or a half-word.

Support for this disclosure can be found throughout the specification. For example, the specification on page 3 at lines 1-3 states,

> In addition, this method and computer program should be able to simply extract *individual arithmetic flags for individual data items* when necessary. (Emphasis added).

Thus, the specification discloses extracting individual arithmetic flags for individual data items. Further, on page 9 at lines 3-17 the specification states,

> Still referring to FIG. 3, processing begins in operation 200 and immediately proceeds operation 210. In operation 210, a field size is determined on which to base the extraction or combination function. **The field size may be, but not limited to, a nibble, byte, half word, word, or double word in size**. The extraction and/or combination function may include any of the foregoing 16 items discussed or any other function which may describe or combine the status or result of a mathematical operation performed by a computer or processor. Thereafter, processing proceeds operation 220 where it is determined if an extraction process is being performed. If an extraction process is being performed processing then proceeds operation 230. **In operation 230, the flags, illustrated in FIGs. 1A through 1D, are extracted based upon the field size determined in operation 210 and the specific data item desired.** Thereafter, processing proceeds operation 270 where the extracted information is stored in the destination register. Once stored processing proceeds to operation 280 where processing terminates. **In an example embodiment shown in FIG. 6, the extraction process is further detailed** as discussed ahead. (Emphasis added).

This portion of the specification discloses that the flags, as illustrated if FIGs. 1A through 1D, may have a field size including but not limited to nibble, byte, half word, word, or double word, and also that any of these may be extracted based upon the field size determined in operation 210 and the **specific data item desired**. Attention is also drawn to the fact that above quoted portion of the specification states that FIG. 6 is an example embodiment of the extraction process. As further disclosed in the specification on page 5 at lines 1-4,

> FIG. 1A through 1D are representative examples of SIMD words utilized to indicate the *arithmetic flags associated with data items* being manipulated by a processor having SIMD capability in the example embodiments of the present invention. (Emphasis added).

Further, the specification on page 5 at lines 17-22 states,

> Referring to FIG. 1A, eight sets of arithmetic flags (120, 125, 130, 135, 140, 145, 150 and 155) are shown in which *each set of flags is associated with an individual data item.* Therefore, the first set of flags composed of N, Z, C, and V is associated with the first data item 120 while the second 125, third 130, and fourth 135 through eighth 155 are associated with the first, second, third, and fourth through eighth data items further illustrated in FIG. 2 and discussed ahead. (Emphasis added).

Thus, FIGs. 1A through 1D disclosure arithmetic flags associated with data items, wherein each set of flags is associated with an individual data item. In a further disclosure related to FIG. 2, the specification on page 6 at lines 15-18 states,

> FIG. 2 is a systems diagram of an example embodiment of the present invention. As illustrated in FIG. 1B, arithmetic flags 120, 125, 130 and 135 are shown in FIG. 2. However, in addition *arithmetic flags 120, 125, 130 and 135 are each associated with data items 100, 105, 110 and 115 respectively.* (Emphasis added).

FIG. 2 illustrates that the groups of arithmetic flags as shown for example in FIG. 1B are each associated with a data item. Thus, the specification discloses extracting arithmetic flags associated with a specific data item, wherein the extraction is based on

field size and the specific data item desired. Therefore, the specification discloses an extraction wherein based on the determined field size, a plurality of specified destination register bits in a destination register are set to the arithmetic flags associated with a selected and specific data item.

Further, the specification in describing FIG. 6 on page 12 at lines 23-24 refers to "the data field illustrated in FIG. 1A for the SIMD word is four bits (one nibble) in length," and on page 13 at lines 9-10 states, "If the data field in the SIMD word is eight bits in length, as shown in FIG. 1B, then processing proceeds to operation 540." In further reference to FIG. 6, the specification on page 13 at lines 16-17 states, "If the data field in the SIMD word is 16 bits in length, then processing proceeds to operation 560."

Thus, the specification clearly associates the data fields and their associated field length in FIG 1A, 1B, and 1C with the extraction illustrated in FIG. 6.

Applicant therefore has amended the specification in the three paragraphs beginning on page 12, line 20 through page 13, line 21 to correct the language associated with operations 520, 540, and 560 of FIG. 6.

With respect to operation 520, the specification has been amended on page 13 at lines 2-3 to read,

> In operation 520, bits 31 through 28 of the destination register are set equal to one of selected nibbles 7 through 0 of the SIMD PSR register.

FIG. 1A has been amended to merely to label the sets of arithmetic flag groups 120, 125, 130, 135, 140, 145, 150, and 155 as nibble 7, nibble 6, nibble 5, nibble 4, nibble 3, nibble 2, nibble 1, and nibble 0 respectively. FIG. 6 has also been amended at block 520 to indicate "DESTINATION REGISTER (31:28) = ONE OF SELECTED SIMD PSR REGISTER NIBBLES (7:0)"

With respect to operation 540, the specification has been amended on page 13 at lines 9-10 to read,

> In operation 540, bits 31 through 24 of the destination register are set equal to one of selected bytes 3 through 0 of the SIMD PSR register.

FIG. 1B has been amended to merely to label the sets of arithmetic flag groups 120, 125, 130, and 135 as byte 3, byte 2, byte 1, and byte 0 respectively. FIG. 6 has also been amended at block 520 to indicate "DESTINATION REGISTER (31:24) = ONE OF SELECTED SIMD PSR REGISTER BYTES (3:0)"

With respect to operation 560, the specification has been amended on page 13 at lines 16-17 to read,

> In operation 560, bits 31 through 16 of the destination register are set equal to one of selected half-words 1 through 0 of the SIMD PSR register.

FIG. 1C has been amended to merely to label the sets of arithmetic flag groups 120 and 125 as half-word 1, and half-word 0 respectively. FIG. 6 has also been amended at block 560 to indicate "DESTINATION REGISTER (31:16) = ONE OF SELECTED SIMD PSR REGISTER HALF-WORDS (1:0)"

Applicant believes that based on the disclosure provided by the specification as originally filed and the drawings as originally filed, no new matter has been added through these amendments to the specification and to FIGs. 1A-1C and FIG. 6. Applicant respectfully requests that these amendments be carefully reviewed in light of the arguments provided above, and that these amendments be accepted.

Further, Applicant believes that these amendments overcome the objections to the specification raised on page 2 of the Final Office Action, and therefore requests that these objections be withdrawn.

Drawings

The Final Office Action on page 3 objected to FIG. 6 for minor informalities. Applicant have included with this response proposed amendments to FIG. 6 which Applicants believe overcome the objections to FIG. 6 raised on page 3 of the Final Office Action. Specifically, blocks 520, 540, and 560 of FIG. 6 have been amended to correspond to the amendments made to the specification relating to blocks 520, 540, and 560. These amendments to FIG. 6 include the following:

The proposed amendment to block 520, wherein block 520 as amended reads,

"DESTINATION REGISTER (31:28) = ONE OF SELECTED SIMD PSR REGISTER NIBBLES (7:0)"

The proposed amendments to block 540, where block 540 as amended reads,

"DESTINATION REGISTER (31:24) = ONE OF SELECTED SIMD PSR REGISTER BYTES (3:0)"

The proposed amendments to block 560, wherein block 560 as amended reads,

"DESTINATION REGISTER (31:16) = ONE OF SELECTED SIMD PSR REGISTER HALF-WORDS (1:0)"

For at least the reasons stated above with respect to the objections to the specification, no new matter has been added through the amendments to FIG. 6.

In addition, proposed amendments have been included with the response for FIG. 1A, FIG. 1B, and FIG. 1C. These amendments merely include descriptive labels numbering the nibbles, bytes, and half-words illustrated in FIG. 1A, FIG 1B, and FIG. 1C respectively, as already described in the specification as noted above. For at least the reasons stated above with respect to the objections to the specification, no new matter has been added through the amendments to FIG. 1A, FIG. 1B, and FIG. 1C.

Applicant respectfully requests that the proposed amendments to FIGs. 1A-1C and FIG. 6 be reviewed and accepted, and that the objection to the drawings raised on page 3 of the Final Office Action be withdrawn.

Claims Objections

Claims 1, 7, 12, and 17 were objected to because the examiner is unclear on why "the plurality of arithmetic flags represent the status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items."

Claims 1, 7, 12, and 17 each recite,

> wherein the plurality of arithmetic flags represent the status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items.

Attention is directed to the specification on page 2, lines 3-15 states,

> A further development created in order to enhance processor performance is the use of a technique known as single instruction multiple data (SIMD). SIMD is a technique where several different pieces of data may be simultaneously accessed and arithmetically manipulated by a processor. This ability to manipulate several pieces of data at the same time greatly enhances the performance of the processor. However, even though the same arithmetic operation may be performed, **the results and status for each piece of data may be different**. For example, the data may be negative, zero, have a carry out or overflow condition resulting. Since a SIMD processor may manipulate as many as eight pieces, or more, of data simultaneously, **the processor is required to maintain at least eight sets of these condition flags**. Further, in order to receive the benefit of SIMD processing it is necessary to logically combine these condition or arithmetic flags so that the appropriate operation may occur under the appropriate conditions.

Thus, the specification discloses that the results and status for each piece of data may be different, and that the processor is required to maintain at least eight sets of these condition flags, wherein each of the eight sets of condition flags would represent the results and status for each piece of data. Based on at least this disclosure from the specification, Applicant believes that the recitation in claims 1, 7, 12, and 17 is not unclear, and respectfully requests the withdrawal of the objection raised on page 3 of the Final Office Action to claims 1, 7, 12, and 17.

Applicant has amended claims 1, 7, 12, and 17 as suggested on page 4 of the Final Office Action in order to provide an antecedent basis for "status." Applicant believes these amendments overcome the objections to claims 1, 7, 12, and 17 raised on page 4 of the Final Office Action, and respectfully requests withdrawal of these objections to claims 1, 7, 12, and 14.

§102 Rejection of the Claims

Claims 1- 4, 6- 9, and 17- 22 were rejected under 35 U.S.C. § 102 (e) as being anticipated by Wilson (U.S. 6, 530, 012) (hereinafter "Wilson").

Applicant believes that claims 1-4, 6-9, and 17-22 are not anticipated by Wilson because Wilson fails to teach each of the elements included in claims 1-4, 6-9, and 17-22.

For example, claim 1 as now amended recites,

> a combination function module that examines a plurality of arithmetic flags, determines field size of the plurality of arithmetic flags and based on the determination of the field size will **logically combine the plurality of arithmetic flags into a single combined arithmetic flag variable**, wherein the plurality of arithmetic flags represent a status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items. (Emphasis added).

There is no disclosure in Wilson of "logically combining the plurality of arithmetic flags into a single combined arithmetic flag variable, wherein the plurality of arithmetic flags represent a status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items," as recited in claim 1. In contrast, Wilson at column 4, lines 43-45 states,

> The general purpose registers also include a condition code register (CCreg) and a test register TSTreg which are discussed in more detail in the following.

With regards to the condition code register, Wilson at column 7, lines 48-55 states,

> A condition code generator 48 also examines the results of each addition and generates condition codes for the side of the machine where the instruction is being executed to be held in the condition code register CCreg. The condition generator 48 always generates eight condition codes for each side of the machine regardless of the degree of packing of the source operands, as described more fully in the following.

And further, Wilson at column 7, line 60 through column 8, line 1 states,

> The condition code generator 48 generates condition codes CCX0 to CCX7 **by considering the results of the addition operations which were carried out on each packed object in the source registers** and determining from those operations the values of N,Z,C and V which are the bits defining each condition code. In the example of FIG. 6, a different condition code can be generated for each condition code location CCX0 . . . CCX7 in the condition code register. (Emphasis added).

Thus, Wilson discloses a condition code register wherein a code generator generates condition codes by considering the results of addition operations carried out on each packed object in the source register. However, there is no teaching in Wilson of logically combining any of these generated results with any other of the results. Thus, Wilson fails to teach "**logically combine the plurality of arithmetic flags into a single combined arithmetic flag variable**, wherein the plurality of arithmetic flags represent a status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items," as recited in claim 1. Thus, Wilson fails to teach each of the elements recited in claim 1, and therefore claim 1 is not anticipated by Wilson.

In further examples of elements recited in the claims and not taught by Wilson, claims 7 and 12 as now amended each recite,

> **logically** combining the plurality of arithmetic flags based on a function selected when a combination process is selected (Emphasis added).

For reasons analogous to those discussed above with respect to claim 1, Wilson fails to teach "logically combining the plurality of arithmetic flags based on a function selected when a combination process is selected," as recited in claims 7 and 12. Thus, Wilson fails to teach each of the elements recited in claims 7 and 12, and therefore claims 7 and 12 are not anticipated by Wilson.

In a further example of elements recited in the claims and not taught by Wilson, claim 17 as now amended recites,

> extracting the plurality of arithmetic flags based on the field size, the plurality of arithmetic flag associated with a single selected data item; and
>
> storing a result of the extracting of the plurality of arithmetic flags in a destination register for access by the processor.

Applicant's representatives are unable to find in Wilson a teaching of these elements as recited in claim 17 and as quoted above. Thus, Wilson fails to teach each of the elements recited in claim 17, and therefore claim 17 is not anticipated by Wilson.

Claims 2-4 and 6 depend from claim 1, and so include all of the elements recited in claim 1. Claims 8-9 depend from claim 7, and so include all of the elements recited in claim 7. Claims 13-14 depend from claim 12, and so include all of the elements recited in claim 12. Claims 18-19 depend from claim 17, and so include all of the elements recited in claim 17. For at least the reasons stated above with respect to claims 1, 7, 12, and 17, and the additional elements included in claims 2-4, 6, 8-9, 13-14, and 18-19, these claims are also not anticipated by Wilson.

In an example of additional elements recited in dependent claims and not taught by Wilson, claims 6, 11, and 16 include a detailed listing of the status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items. Wilson fails to disclose these elements as recited in claims 6, 11, and 16.

In an attempt to supply these elements missing from Wilson, the Final Office Action on pages 7-10 refers to Table 1 in column 6 of Wilson. However Wilson at column 5, line 62 through column 6, line 7 states,

> The 8-bit field of each Treg is as shown in FIG. 4. The Condition field (bits 0 to 3) applies to all predicated instructions. It holds a 4 bit test code to allow for conditions to be tested. As discussed in more detail later, for instructions on packed objects, the condition applies to all the lanes on a per lane basis. The four condition flags are: N (Negative flag--bit 3) Z (Zero flag--bit 2) C (Carry flag--bit 1) V (Overflow flag--bit 0) **These four bits give rise to 16 test conditions** (see Table 1).
> (Emphasis added).

Thus, Table 1 of Wilson discloses test conditions associated with FIG. 4. FIG. 4 represents a test register Treg, and therefore, any "test conditions" described in Table 1 of Wilson relate to a test register. Wilson describes how these test conditions are set at column 5, lines 50-53 which states,

> The Treg bytes are programmable and are set to the required values prior to instruction execution. The test register is used to allow conditional execution of instructions.

Thus, these bytes in test register Treg and referred to in Table 1 are programmable and set to the required values prior to instruction execution. However, there is no disclosure in Wilson that teaches a status associated with a plurality of data items after a mathematic operation is performed by the processor on the plurality of data item, as recited in claims 6, 11, and 16. Therefore, Wilson fails to disclose these additional elements, and so fails to anticipate claims 6, 11, and 16.

Applicant respectfully requests withdrawal of the 35 U.S.C. § 102 (e) the rejection claims 1- 4, 6- 9, and 17- 22, and reconsideration and allowance of all claims pending in the application.

§103 Rejection of the Claims

Claims 5, 10-11 and 15-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wilson in view of Bindloss et al. (U.S. 5, 778, 241).

Claim 5, which is dependent from claim 1, includes all of the elements of claim 1, and is therefore patentable over Wilson for at least the same reasons as stated above for claim 1. Bindloss et al. does not supply the elements of claim 1 which are missing from Wilson. Thus, the proposed combination of Wilson and Bindloss et al. fails to teach or suggest each of the elements included in claim 5.

Claim 10-11, which are dependent from claim 7, include all of the elements of claim 7, and are therefore patentable over Wilson for at least the same reasons as stated above for claim 7. Bindloss et al. does not supply the elements of claim 7 that are

missing from Wilson. Thus, the proposed combination of Wilson and Bindloss et al. fails to teach or suggest each of the elements included in claims 10-11.

Claim 15- 16, which are dependent from claim 12, include all of the elements of claim 12, and are therefore patentable over Wilson for at least the same reasons as stated above for claim 12. Bindloss et al. does not supply the elements of claim 12 that are missing from Wilson. Thus, the proposed combination of Wilson and Bindloss et al. fails to teach or suggest each of the elements included in claims 15-16.

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection, reconsideration and allowance of claims 5, 10-11, and 15-16.

New claims 23-25

Applicant submits that new claims 23-25 are distinguishable and thus patentable over the Wilson and Bindloss et al. documents, both when these documents are taken alone or in combination. Applicant respectfully requests allowance of new claims 23-25.

Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at 612-371-2132 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

NIGEL C. PAVER

By his Representatives,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, Minnesota 55402
612-373-6900

Date OCTOBER 3, 2007 By Robert B. Madden
Robert B. Madden
Reg. No. 57,521

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop PETITIONS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 3rd day of October, 2007.

Amy Moriarty
Name

Signature